

## Apple II Hardware: 6522 Versatile Interface Adapter (2/97)

Revised: 3/3/97 Security: Everyone

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TOPIC -----

This article describes the 6522 Versatile Interface Adapter (6522 VIA).

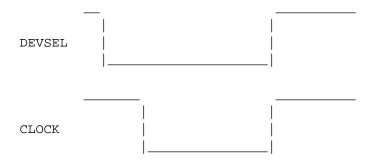
DISCUSSION -----

The 6522 Versatile Interface Adapter (6522 VIA) is a popular integrated circuit for use with microcomputers because it operates in a variety of modes. The precursor to the 6522, the 6520, has been used in several interfaces with no difficulty. Unfortunately, although these two parts have identical timing specifications, their operation is different. The 6520 is very tolerant of operation outside of the parameter limits on its data sheet while the 6522 must have its timing specifications met exactly.

The most critical timing parameter for the 6522 is the address set-up time, the delay between the chip select and the rising edge of the 1MHz clock. The 6522 will not operate under the nearly identical Device Select and 1 MHz clock of the Apple II. The solution is to shorten the positive half-cycle of the 1 MHz waveform. This can be achieved by various methods, but, since the length of the positive half-cycle is critical, it is essential to have a well-controlled circuit to do this.

The circuit below is proposed for use with the Apple II. The 74LS74 circuit delays the positive edge of the clock by one cycle of the 7 MHz clock, generating the clock waveform that the 6522 needs. The negative edge of the clock is set by the falling edge of the 1 MHz clock; this also holds off the flip-flop until the next cycle. The shortened positive half-cycle of the clock waveform results in a leading edge delayed by 140 nanoseconds from the falling edge of Device Select.

The 6522A is required to meet the data sheet timing parameters. The 6522 will usually work but its operation cannot be guaranteed.



## SUGGESTED SCHEMATIC

(25) +5	<del>+</del>		+·	+
(40) Q0		74LS74	10   2 9	+
(36) 7M+-   - 	  3     1	   1: 	1   	
(41) DEVSEL				
(18) R/W	_     11 9	- 	24	
(42) D7 (43) D6 (44) D5	18 2	L   2   3	27	   
(45) D4 (46) D3 (47) D2	15 0 5	1	30 6	   
(48) D1 (49) D0	•	7   3	!	I/O   Lines:   Port A
( 5) A3 ( 4) A2			35  36 2	     and 
( 2) A0( 31) RESET			38 A  34	   Port B   
(30) IRQ				

Article Change History:

28 Feb 1997 - Reviewed for technical accuracy, revised formatting.

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