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Asynchronous DataComm (Stop Bits and Framing Errors)

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BACKGROUND

In RS232 there are two data pins, one for transmit and one for receive. One of two possible voltages on a data wire will express the state of the bit being transferred. In RS-232 the logic zero is assigned the positive voltage and the logic one is assigned the negative voltage.

When no data is being transferred on the data wire it is considered to be in an idle condition. In the idle condition the data wire has the same voltage that is used to express a one.

Inside both the transmitting and receiving units are electronic devices called clock circuits, which produce signals called "clock pulses" or clocks. The frequency of the clock signal is dependent on the BPS or Baud rate being used for the transmission. In synchronous data transfers, clock signals accompany the data being transferred.

In asynchronous data transfers, clock signals are used only on the "inside" of the sending and receiving units. This article discusses asynchronous data transmission only.

To make it easy for the receiving unit to know how many bits are coming, every asynchronous data transfer contains a set number of bits. Each transfer contains one byte of data plus a start bit and one or more stop bits.

START BIT

In an asynchronous data transfer, the receiving unit needs a change in voltage on the data wire to notify it that data is coming. The sending unit does this by preceding every character transmitted with a start bit (a logic zero; positive voltage in RS-232). After the sending unit does this it uses eight clock pulses to clock eight bits on to the data wire.

Once the receiving unit senses the start bit, it knows that data will follow. So, it clocks the data in from the data wire.

STOP BIT

In asynchronous data transfers the receiving unit will always wait a period of time after the eighth bit is clocked in before it will again allow itself to detect a start bit on the data wire. This period is divided into bit times, the same length as those used for the transmitted data bits. Since they signify the end of the character transmission, these bit times are called stop bits.

The number of stop bits (usually one or two) can often be selected when configuring application software, interface boards, and DIP switches. If all three places give the option for selecting stop bits, they should all be set to the same value. During the stop bit, the sending unit should maintain the data wire at the negative (idle) voltage level. At this time, the receiving unit will sample the data wire.

If both the sending unit and receiving unit are at the same BPS (BAUD) rate, then after it has finished clocking in the data from the sending unit, the receiving unit should see the stop bit's negative (idle) voltage level.

If the receiving unit sees a positive voltage at this time, then it knows that it and the sending unit are out of synchronous so it generates a framing error.

NOTE: A framing error commonly occurs when the sending and receiving units are at different BPS or BAUD rates.

CHARACTER MODE ASYNCHRONOUS

Character mode asynchronous data transfers occur one byte (character) at a time, with each transfer separated by idle time. Character mode is used for interactive communications, as when a personal computer user in terminal mode communicates with a bulletin board.

BLOCK MODE ASYNCHRONOUS

Block mode asynchronous data transfers have no idle time between character transmissions. The sending unit packs the asynchronous data transfers end to end with no idle time (except for the stop bit). A block mode asynchronous data transfer is used for things like file transfers, where a large mass of already existing data is sent.

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