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Macintosh IIfx: Latched Writes

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TOPIC ----------

This article describes Macintosh IIfx latched writes.

DISCUSSION ----------

The Macintosh IIfx supports zero wait-state writes to memory by using 64-pin SIMM strips and the new memory-controller technique of latched writes. When the processor issues a write, the memory controller saves the data in a temporary location (the latch, hence the name latched write) and tells the CPU the write has finished (even though it isn't. It lies). The CPU is then free to execute the next instruction. The memory controller then takes data and does a normal write operation. If more data is written out in the next cycle, Page Mode Access is used to write the remaining data.

There are three phases of a latched write. These phases are:

1) The processor writes out the data.

2) The FMC (Fast Memory Controller) stores the data in the latch and tells the processor the write was completed successfully. The 68030 is now free to execute the next instruction.

3) The FMC then writes the data from the latch into system DRAM.

On a normal SIMM strip, the "D In" lines and the "Q Out" lines are tied together. Using 64-pin SIMMs, these lines can be separated and you can have data going in, while using the output bus of the SIMM at the same time. This lets the memory controller implement latched writes and provide zero wait-state writes.

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