Fast Page DRAM: A Description

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TOPIC ----------

This article describes fast page DRAM and compares it with ordinary DRAM.

DISCUSSION ----------

A dynamic random access memory (DRAM) chip consists of one-bit memory cells organized in rows and columns. Each memory cell is a capacitor. This capacitor is either charged or discharged to represent a high or low state, respectively. The design's advantage is it allows very high-density memories by requiring only one transistor per bit.

However, this design has a timing bottleneck. Since the amount of stored charge is very small, it must to be amplified before being placed on the data bus. This results in a 80 to 120 nS access cycle time. However, there are methods to minimize the affect of this overhead.

With a basic DRAM design, two signal lines are alternatively strobed back and forth to access the data within the DRAM, because the address lines are shared. These signal lines are Column Address Strobe (CAS) and Row Address Strobe (RAS). The access sequence is as follows: put the row address on the bus, assert RAS, put the column address on the bus, assert CAS and then get the data.

Page DRAM has a timing sequence that eliminates the need for multiple RAS strobes when accessing data within the same row. When the chip sees one RAS strobe, multiple address and CAS strobes access the data in the same row. This type of memory access is beneficial for burst mode accesses. The first read takes the usual overhead, because one set of RAS and CAS strobes must be initiated. However, subsequent reads are shorter because the RAS line does not have to be asserted again for each data request.

Basically, fast page mode DRAM is a page DRAM with slightly different logic that allows for an even faster access time. Transparent latches are used for immediate access to the data. These latches make the data available even before the latch locks in the data. It is this additonal speed that allows the "5-2-2-2" cache burst mode on the Macintosh IIci to work.

This burst mode allows the use of cost-effective DRAMs, while providing high performance. The 68030 has a four long word cache (16 bytes), which is quickly filled by the "5-2-2-2" cycle. The processor accesses data from the cache subsequently until a cache miss. Then another "5-2-2-2" cycle is done.

Fast page mode DRAM has a little more logic than a basic DRAM chip, but permits fast access to sequential data within a column at speeds required for the Macintosh IIci.

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