

## Tech Info Library

## Workgroup Server 9150: Memory Overview (4/94)

Revised:	4/26/94						
Security:	Everyone						
Workgroup Serve	er 9150: Memory Overview (4/94)						
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Article Created	l: 26 April 1994						
TOPIC							
This article pr	rovides a memory overview of the Workgroup Server 9150 (WS 9150)						
DISCUSSION							
The Workgroup S	Gerver 9150 computer's memory is organized in three levels:						

- Internal cache
- External second level cache
- Main memory array

Access to data or instructions in memory, including routine copy back and refill maintenance is controlled by hardware. The main memory array is buffered from the cached bus so that external second level cache operations can proceed simultaneous with video refresh, I/O DMA, and other operations.

All memory operations are controlled by the High speed Memory Controller (HMC) ASIC.

Workgroup Server 9150 supports a single 32 bit memory map. Virtual memory is supported through the PowerPC 601 processor's internal memory management unit. The physical memory map is shown below. Of course the logical memory map is up to the discretion of the system programmer and may be configured to provide a Macintosh compatible 24 bit address space.

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		EMI	PTY	I

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